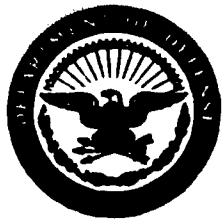
AD 294 663



REPRODUCTION QUALITY NOTICE

This document is the best quality available. The copy furnished to DTIC contained pages that may have the following quality problems:

- Pages smaller or larger than normal.
- Pages with background color or light colored printing.
- Pages with small type or poor printing; and or
- Pages with continuous tone material or color photographs.

Due to various output media available these conditions may or may not cause poor legibility in the microfiche or hardcopy output you receive.

☐ If this block is checked, the copy furnished to DTIC contained pages with color printing, that when reproduced in Black and White, may change detail of the original copy.

U. S. NAVAL AIR DEVELOPMENT CENTER

JOHNSVILLE, PENNSYLVANIA

Aeronautical Electronic and Electrical Laboratory

REPORT NO. NADC-EL-6272 18 DEC 1962

FREQUENCY SYNTHESIZER
A METHOD OF FREQUENCY CONTROL
BY DIGITAL CONVERSION

FOUNDATIONAL RESEARCH REPORT
WEPTASK NO. R360FR102/2021/R011-01-01
Task No. FR40-3-03(6105A)

SUMMARY

A study was initiated to develop a frequency synthesizer to replace present day spectrum generators. The design objectives were to minimize spurious signal outputs, eliminate mechanical components, and to incorporate electronic circuitry compatible with micro-miniaturization techniques.

A method of frequency control was developed, using counters and logic circuits to develop a highly accurate coded error to connect to a variable frequency oscillator. A breadboard model was constructed, which was capable of preselecting any discrete frequency within the range from 2.0 to 3.0 mc with a theoretical accuracy of ±1 count.

It was not possible to obtain the design goal accuracy of ±1 count because of the poor short-term stability of the voltage-tuned variable-frequency oscillator and excessive phase shift in the counter circuits. This study, however, proved the feasibility of using digital computer logic in frequency synthesizer design, and it is recommended that this technique be incorporated in future equipments.

Utilizing present day modular components and optimized package density, the overall size and power consumption would be too great for a practical application in airborne equipment. However, the entire system may readily be replaced by micro-miniaturized circuitry.

The frequency control techniques generate an output signal from a single vfo which minimizes the generation of spurious outputs. By changing only the vfo and mixer stages, these frequency control systems are capable of providing a standard by which it is possible to obtain a band of discrete frequencies over the entire r-f spectrum.

FREQUENCY SYNTHESIZER
A METHOD OF FREQUENCY CONTROL
BY DIGITAL CONVERSION

FOUNDATIONAL RESEARCH REPORT
WEPTASK No. R360FR102/2021/R011-01-01
Task No. FR40-3-03(6105A)

I N T R O D U C T I O N

Task No. FR40-3-03(6105A) was established as a project of the NAVAIR-DEVCEN Foundational Research Program for the investigation of means to reduce interference in airborne communication systems. As a phase of this task, a study was initiated to develop a frequency synthesizer capable of providing a multiplicity of accurate output signal frequencies with a minimum of spurious signals for use in communications and test systems.

Two methods of frequency generation are presently in wide use:

1. Harmonic spectrum generators in which harmonics and sub harmonics of a standard crystal controlled oscillator are mixed together to provide multiple output signals, harmonically related to the standard oscillator.

2. Stablized master oscillators (SMO) in which the frequency of the master oscillator is controlled by reference signals from a harmonic spectrum generator. The output frequency of the master oscillator is harmonically related to the spectrum generator.

The harmonic spectrum generator method results in the generation of unwanted spurious frequencies in the combining mixers. It is a difficult problem to select the desired harmonic while rejecting adjacent undesired harmonics, and requires extensive filtering as channel spacing is decreased (as in SSB systems). The harmonic spectrum generator method often requires mechanical components that are difficult to align and repair in the fleet. Also, the present methods are incompatible with the trend toward use of integrated circuitry which is not presently capable of reproducing tuned circuit elements.

THEORETICAL DISCUSSION

FREQUENCY - DIGITAL CONVERSION

In general, the frequency-digital conversion technique consists of converting frequency to a digital code, comparing the code to a desired frequency code, and developing an error indication that is used in tracking a master vfo. The technique results in the following advantages:

1. The output signal is obtained from a single vfo, which minimizes the generation of spurious outputs.

2. Any single frequency may be selected. It is not harmonically related to a standard frequency source.

3. The use of computer and logic circuits permits adapting this design to micro-miniaturization techniques.

There are two basic means of obtaining frequency control by digital conversion, the open loop (sequential control) method shown in figure 1, and the closed loop (continuous control) method shown in figure 2. Within these frameworks there are several variations by which programming, frequency error, and the digital to analogue error conversion may be determined

Open Loop Method

The output of the vfo is converted to a digital code by means of an exact time gate and counters. Upon completion of the count, the frequency is stored in the counter circuits as a digital code. This code is then compared to the desired preset frequency code of the programmer in a subtractor circuit. The frequency difference is then converted to an error voltage by the digital to analogue converter. This error voltage is fed to a frequency control circuit to track the vfo to the desired frequency upon completion of each cycle. The standard time gate is again opened and the cycle repeated to maintain a sequential control.

Closed Loop Method

The vfo output is fed continuously to the counters which have been programmed to divide by a predetermined number such that the fundamental frequency of the counters is always equal to the frequency standard. The phase detector error output is fed through a low pass filter to the frequency control circuit to track the vfo to the desired frequency. The output of the counters is fed back to the programmer at the instant all counters are reset to zero to initiate the programming cycle. This method used the present SMO frequency control techniques. However, use of the counters as a variable divider permits multiple frequency control.

Comparison of Open Versus Closed Loop

The closed loop method has the advantage of a continuous frequency control to the vfo through a closed feed back loop, and the phase detector eliminates the need for a complex digital to analogue error conversion. However, the standard frequency at the phase detector limits both the number of discrete input frequencies that may be programmed and the minimum channel spacing. For example:

Total division $N = 10^5$ (5 decades)

Frequency standard F_s = 1 kc = 10^3 cps

Highest input frequency to counters Fvfo (max) = N max x F_s = 10^8 cps

= 100 mc

Maximum discrete input frequencies N max = 10^5

Channel spacing = N - (n-1) x F_s = 1 kc (min)

Since present day counters are not capable of input frequencies in excess of 100 mc the maximum discrete frequencies for the above example = 10,000.

The theoretical accuracy of the closed loop method is dependent primarily on the accuracy of the phase detector and the frequency control feed back loop. If the count and programming rate are within the capabilities of the counters the time delay errors will cancel out and the error contributed by the counters alone will be zero. Since the channel spacing is dependent on the frequency standard at the phase detector it would be necessary to use a low reference frequency to obtain close channel spacing. This results in a limited capture range and requires selective filtering. The problem of obtaining high resolution and stability is typical of all closed loop systems.

The open loop method utilizing a 1-sec gate input, may be compared to a closed loop system in which the frequency standard is 1 cps. The decimal counters are capable of storing and programming 10^M - 1 discrete frequencies, where M = the number of decades.

Total division = N = 10^M = 10^8 (8 decades)

Highest input frequency counters = Fvfo (max) = N max x F_s = 100 mc

Maximum discrete input frequencies N max - N min = 100 mc

Channel spacing = 1 cps

The theoretical maximum error of the open loop method is ±1 count due to the unsynchronized vfo count cycle plus the resolution error of the frequency control elements. The higher the vfo frequency the lower the percentage error. It is possible to obtain high error resolution and eliminate the problem of instability in the frequency control loop by use of the digital to analogue conversion.

VARIABLE FREQUENCY OSCILLATOR

There were no attempts made to analyze the design parameters of the vfo. Wide band electronic tuning of the vfo resulted in decreased Q and degradation of the signal to noise power ratio. The counters were capable of determining only the average frequency of the vfo during the count cycle. The problems of short term stability and noise modulation which resulted in the generation of spurious outputs was not within the scope of this investigation.

GENERAL DESCRIPTION

The general block diagram of the breadboard unit, figure 3, embodies the principles of the open loop method previously outlined.

The 1-mc frequency standard is a crystal-controlled oscillator with an accuracy of 2 parts in 10^8. The output of the frequency standard is gated to a set of counters capable of a total division of 10^6. The output of these counters is fed back to the input gate so that an accurate 1-sec gate is generated. The 1-mc standard is also tripled to give an accurate 3.0-mc output.

The vfo is varacter-tuned over a frequency range from 2.0 to 3.0 mc. This output is combined in the mixer with the 3.0-mc frequency from the standard frequency tripler. The difference frequency from the mixer (F standard - Fvfo = F input) is now in the range from 0 to 1 mc. This signal is gated through a variable time gate to a set of programmed counters also capable of a total division $N = 10^6$ (6 decades), which permits 10^6 -1 discrete vfo frequencies to be selected. Before each count cycle, the programmer resets the counter from zero to a frequency count equal to N-F input. After each programming cycle the counters divide by F input = f standard - f vfo. The programmer consists of six 10-position wafer switches connected to the SET inputs of each decade that convert frequency to the digital code compatible with the counter used.

Upon completion of the programming pulse, a start pulse is applied simultaneously to the variable time gate generator and the standard time gate to initiate the counting cycle.

The output of the programmed counters is fed back to determine the width of the vfo gate and therefore equals P input/P desired (P = period). If the input frequency equals the desired frequency, the vfo gate width

is exactly equal to the standard one-second gate. If the input frequency is too low (vfo frequency too high), the vfo gate is longer than one second; and if the input frequency is too high, (vfo low) the vfo gate is shorter than one second. The widths of the standard one-second gate and the vfo gate are compared in a comparator circuit and a high or low frequency error gate is generated. The vfo high frequency error gate applies the input frequency (F in low) to the one-second standard counter line that has completed the count cycle. The exact frequency error can be read out on the upper Nixie lights. If the vfo is below the desired frequency, the low error gate applies the input frequency (F in high) back to the vfo counter line to read out the error on the lower Nixie lights.

The Nixie lights are required only to permit a visual indication of frequency error during the testing phase. However, since the logic circuits that control these lights constitute a binary-coded decimal decoder, the error count is used to control the servo motor to vary the position of the follow-up potentiometers, which in turn determine the varactor voltages of the vfo and output frequency.

PROCEDURES

The breadboard model (figures 4 and 5) was constructed to prove the feasibility of the digital conversion system. No attempt was made to miniaturize the breadboard model, however, transistorized logic modules, consistent with the present state of the art, were used throughout. The detailed block diagram of the entire synthesizer is shown in figure 6.

A total of 12 transistorized decade counters and decoders were required. The counters are capable of a maximum count rate of 2.0 mc. They were not designed for external programming and it was necessary to modify the internal wiring to provide both a set and reset capability. (See figure 7.) The logical 0 level was -6 v and the logical 1 level was 0 v throughout the system. The decimal code for counts 0 to 9 is shown in figure 8. The frequency selection switches, one for each decade, consist of 4 wafers each and are compatable with this code.

The logic circuit was built on 7 plug-in printed boards (figure 5). Commercially available welded modules capable of a 5-mc rate were used wherever possible. Since the logical functions that comprise cards 1 through 6 may be determined from the block diagrams of figure 6, the detailed circuit drawings are not included.

The circuit of card 7, which consisted of the 1-mc, tripler and mixer, and the 0- to 1-mc video amplifier, is shown in figure 9. This circuit, in addition to the vfo and standard oscillators, required tuned circuit elements.

The 1-mc standard was a crystal-controlled transistor oscillator mounted in an oven with an accuracy of 2 parts in 10^8.

The vfo, figure 10, was voltage tuned over the range from 2.0 to 3.0 mc. Two parallel PC-116 varactors were used to obtain sufficient change in the tuned circuit capacitance. The fine control was obtained by a single PC-116 varactor loosely coupled to a tank circuit by a 5-picofarad capacitance. The 25-k follow-up potentiometers controlled the applied negative voltage (-4 to -36 v) to tune the vfo. The follow-up potentiometers were driven by a 400-cps motor, which was controlled through relays by error information from the logic circuit.

The input power was obtained from commercially available modular power supply units as follows:

-18 vdc at 2 amp; counters and logic circuits. (Zenner diodes were used to obtain -12 and -6 v.)

+6 vdc at 100 ma; counters and logic circuits.

+28 vdc at 70 ma; crystal standard and video amplifier.

Total required power = 38 w

+50 vdc at 4 ma; Nixie lights.

+120 vdc at 300 ma; Nixie lights.

Total required power for testing = 36 w

RESULTS

It was not possible to achieve the design goal accuracy of ±1 count in the breadboard model:

1. Modifying the internal wiring of the decade counters to permit programming required extending critical low level signal paths which resulted in erratic operation, particularly in the "units" position. It was necessary to remove this modification so that the breadboard model was capable of programming to ±10 cps only.

2. The time delay (phase shift) through the counters operating with a 1-mc input signal resulted in a +4 count error. To improve the accuracy of the 1-sec gate it would be necessary to compensate for this time delay.

3. The decimal decoder circuit was designed for operation with the Nixie lights. These outputs were modified to provide the error voltages to the varactor controlled vfo. However, decimal decoders capable of providing more accurate weighted output levels exist and would have resulted in improved frequency resolution.

4. The short-term stability of the vfo was extremely poor; averaging at best ±20 cps. This circuit could be improved by proper selection of temperature-compensated components, more stable line voltages, and the addition of oven temperature control. The poor short-term stability of the vfo was the limiting factor in achieving the desired accuracy.

Reported by: C. Halko and J. Rawley
Radio Division

Approved by: H. Vantine, Jr., Superintendent
Radio Division

D. W. Mackiernan
Technical Director

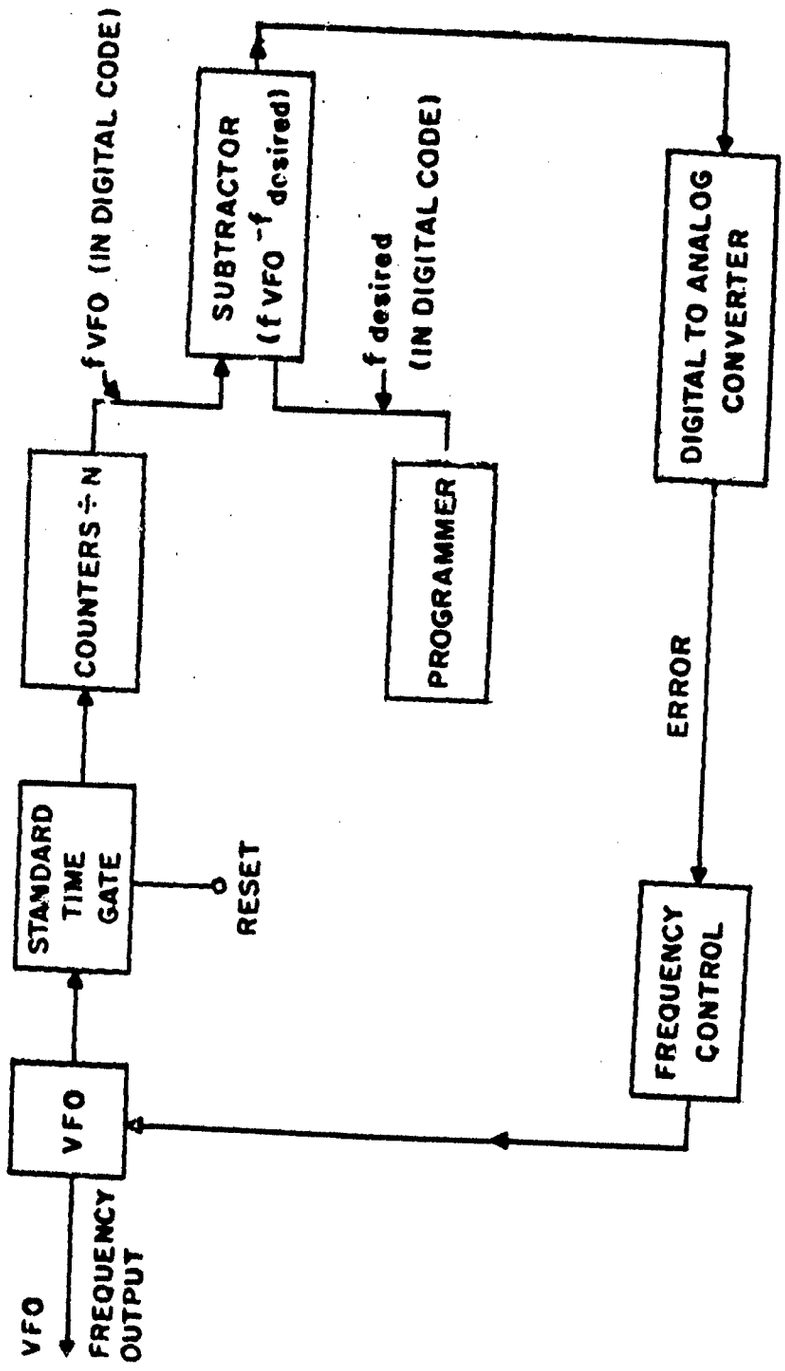


FIGURE 1 - Block Diagram - Open Loop Method

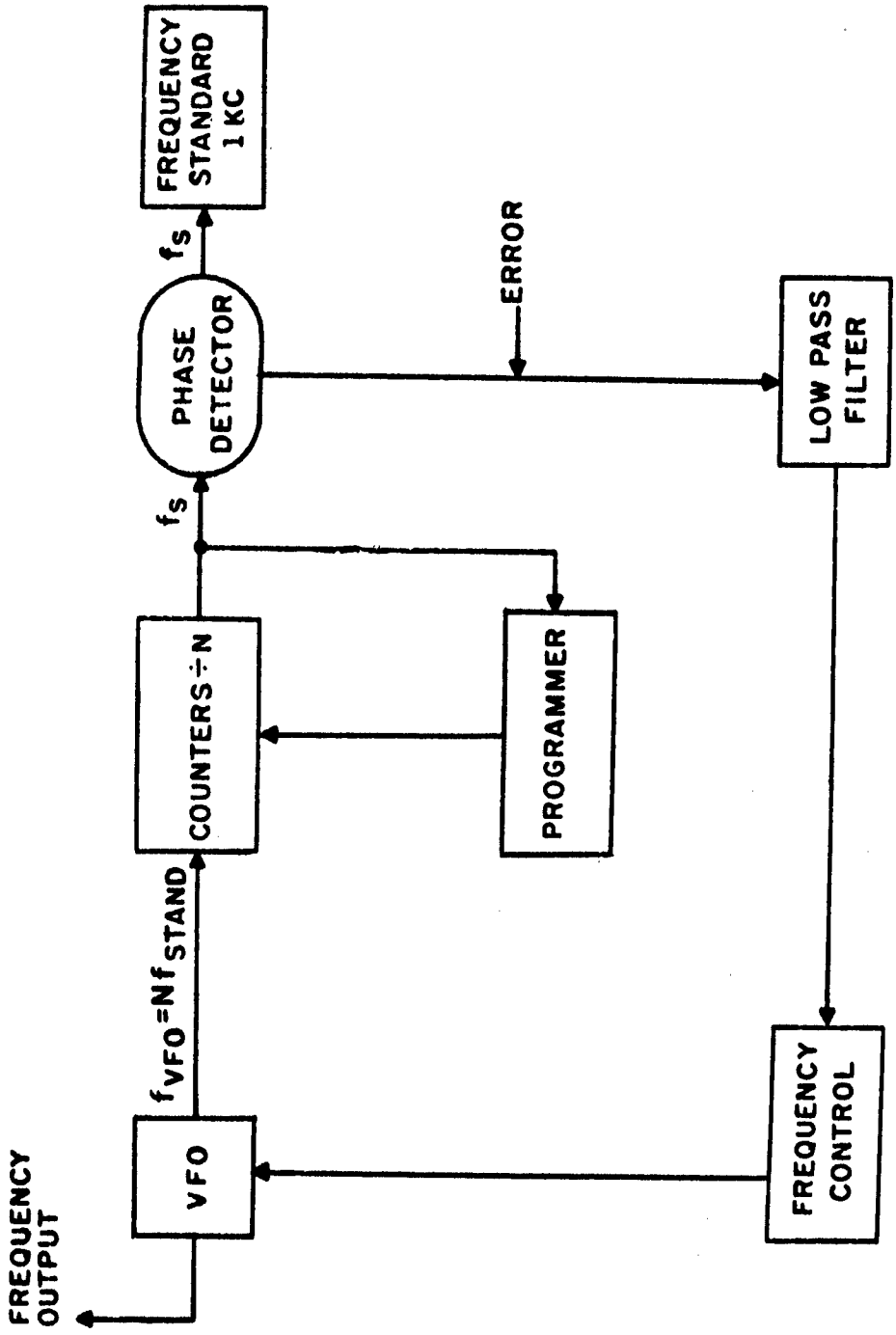


FIGURE 2 - Block Diagram - Closed Loop Method

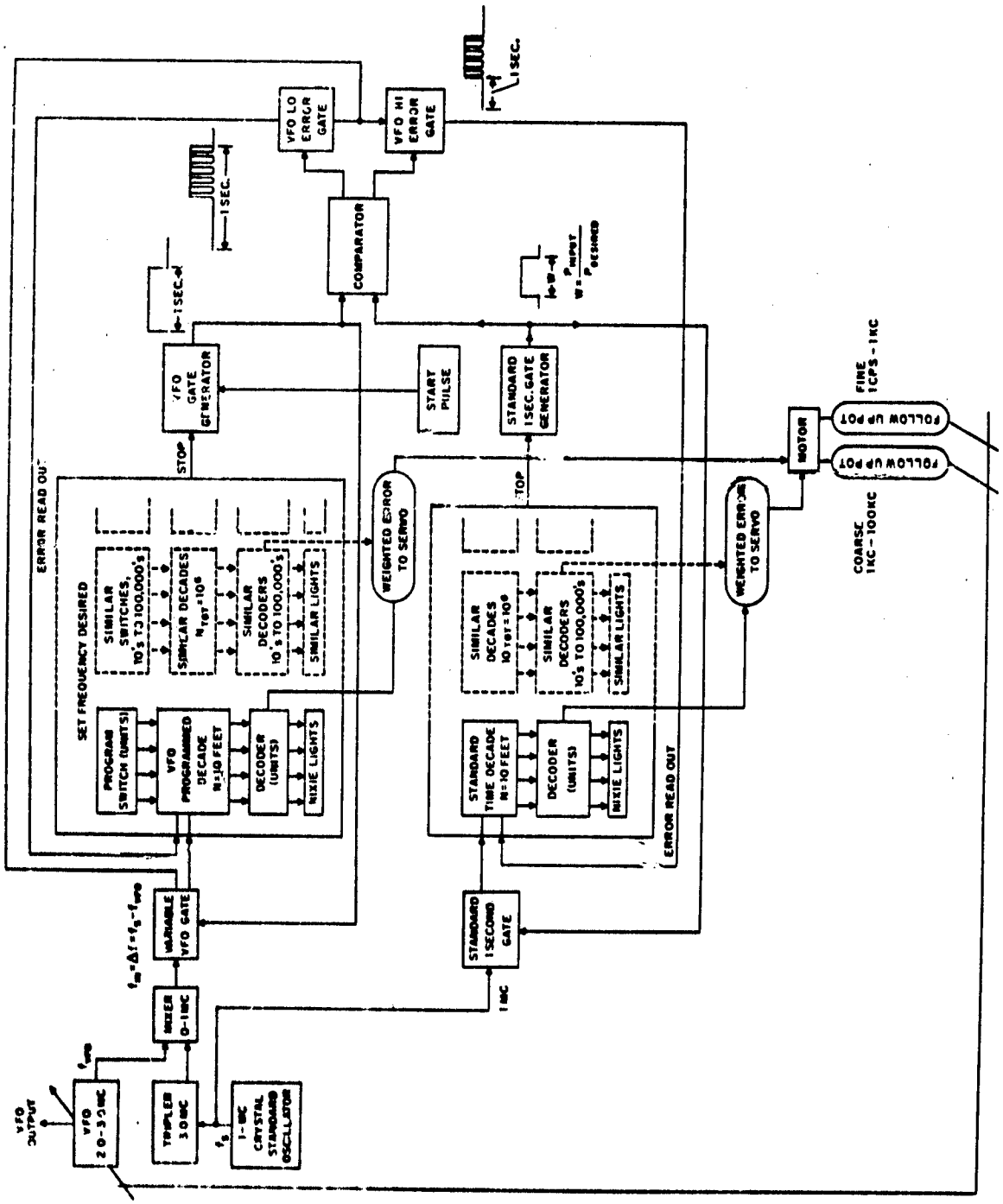


FIGURE 3 - Block Diagram - Frequency Synthesizer

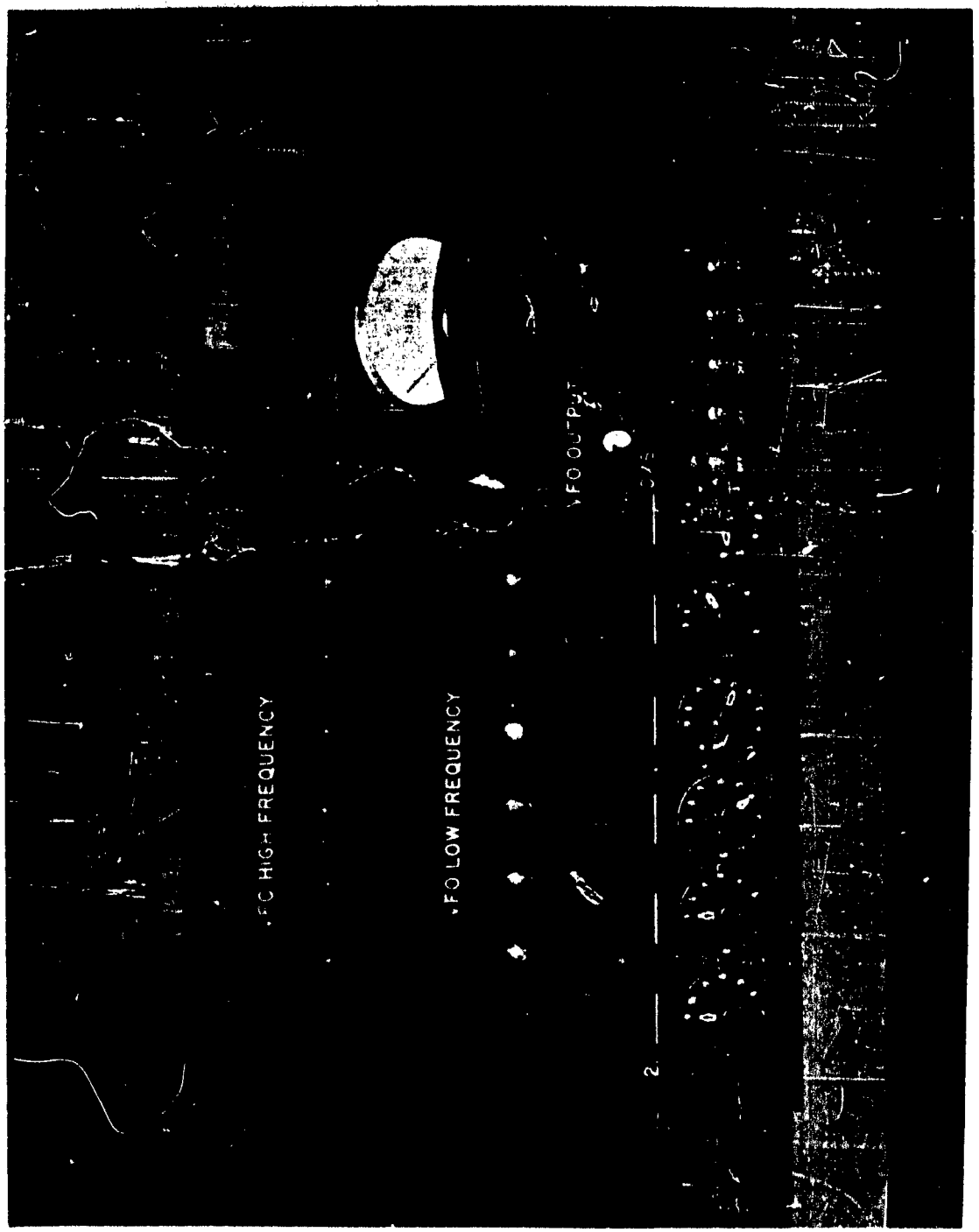


FIGURE 4 - Front View - 2.0 - 3.0 mc Frequency Synthesizer, Breadboard Unit

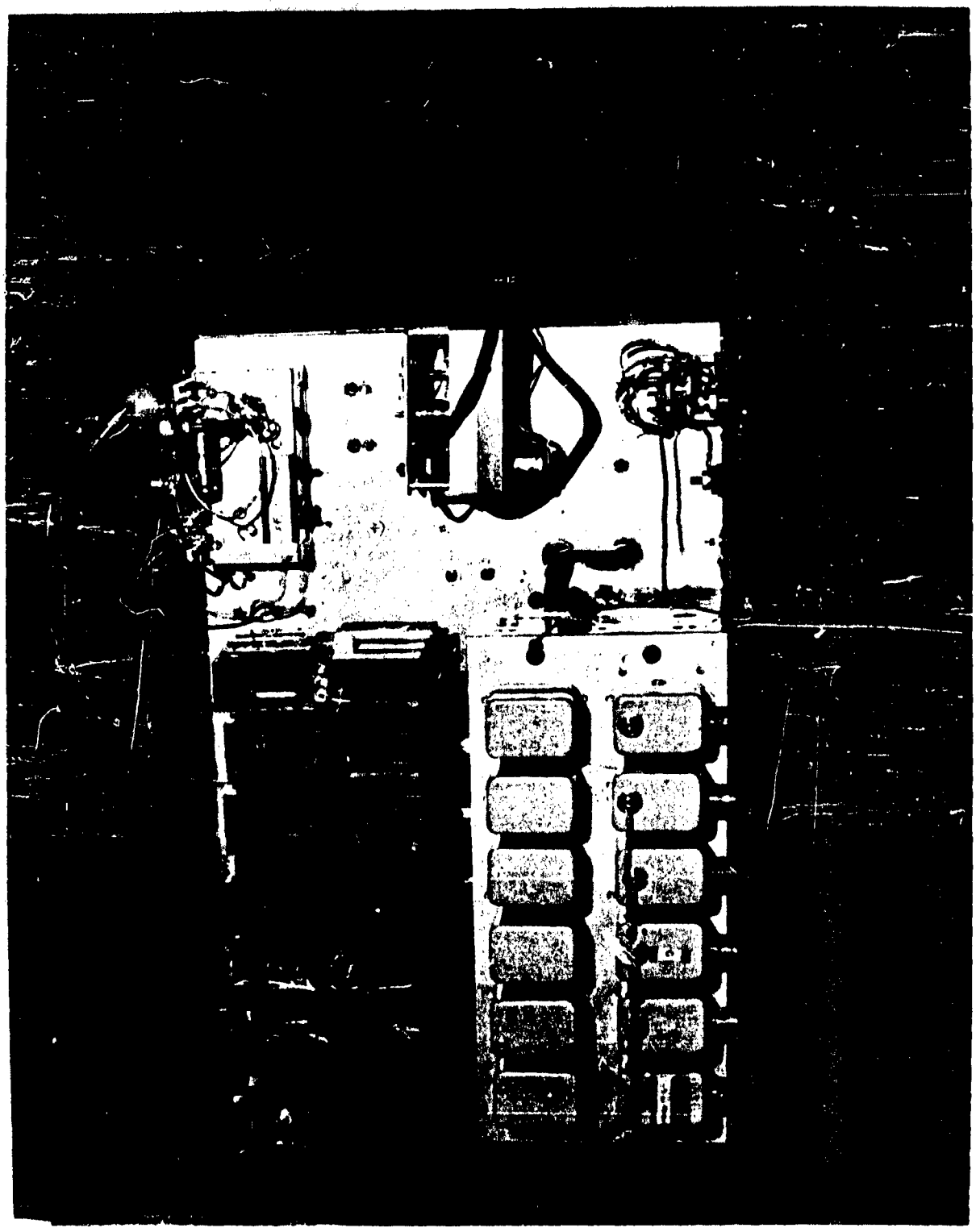


FIGURE 5 - Top View - 2.0 - 3.0 mc Frequency Synthesizer, Breadboard Unit

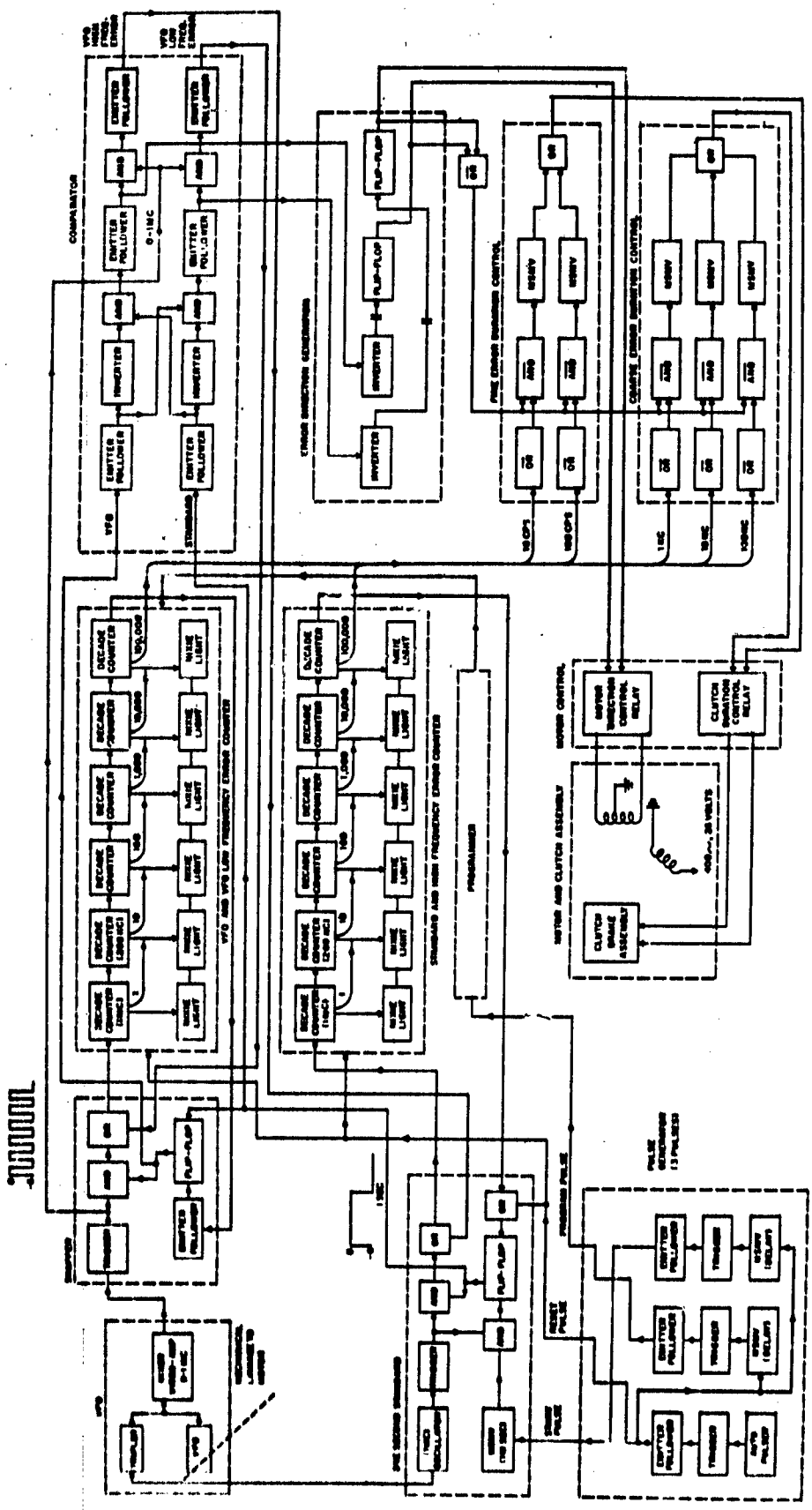


FIGURE 6 - Detail Block Diagram - 2.0 - 3.0 mc Frequency Synthesizer

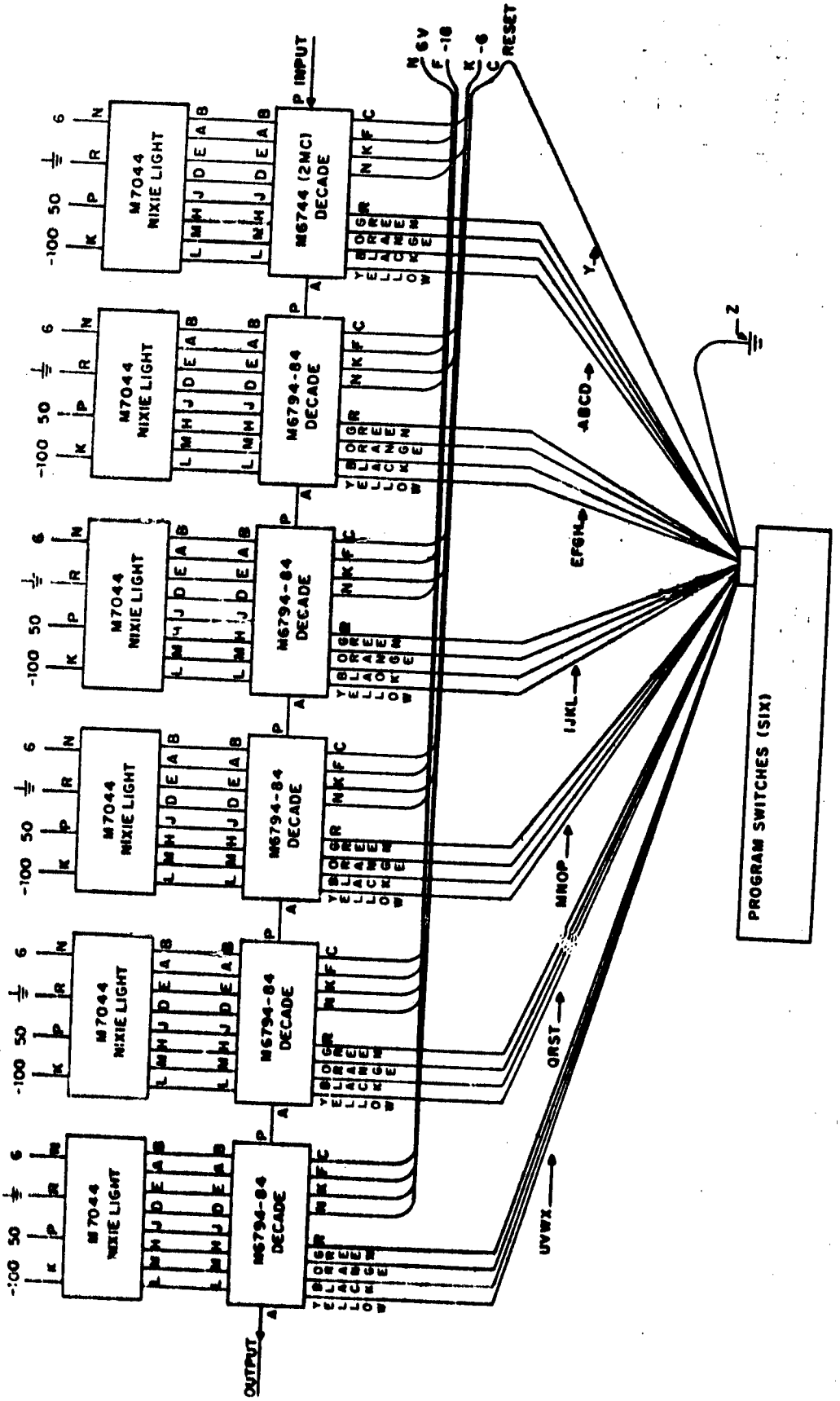
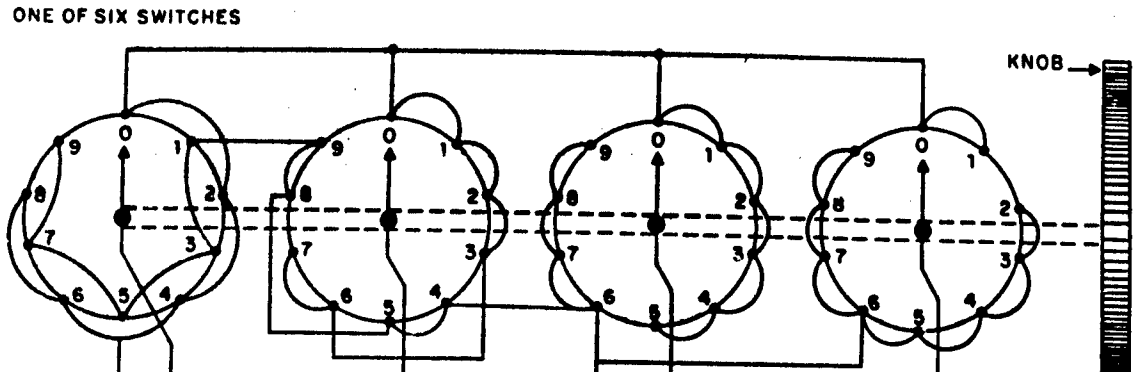
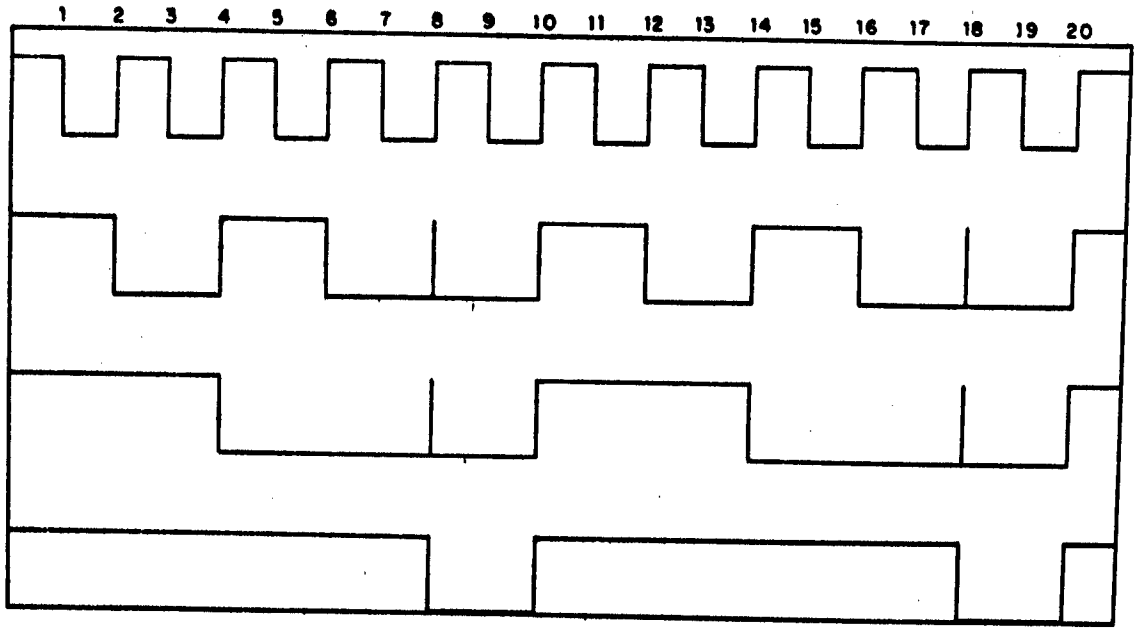


FIGURE 7 - Intercomecting Diagram - Counters and Decoders



DIAL	PROGRAMS	COUNTER CODE
9	0	1111
8	1	1110
7	2	1101
6	3	1100
5	4	1011
4	5	1010
3	6	1001
2	7	1000
1	8	0001
0	9	0000 ← FIRST DIGIT



1 - 1110
2 - 1101
3 - 1100
4 - 1011
5 - 1010
6 - 1001
7 - 1000
8 - 0001
9 - 0000
0 - 1111

FIGURE 8 - Diagram - Frequency Selector Switch and Decimal Code

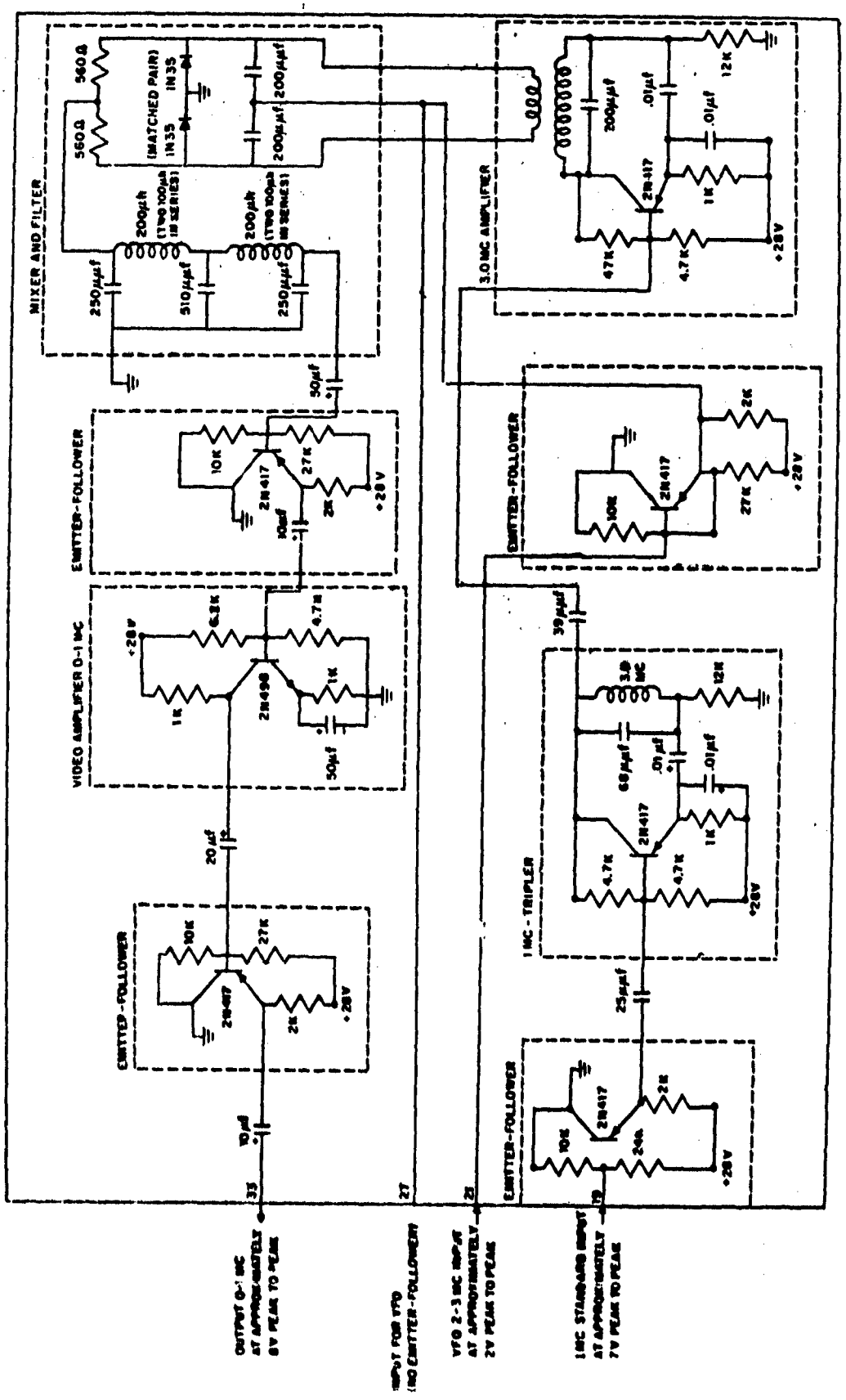


FIGURE 9 - Circuit Diagram Card No. 7 - VFO Mixer and Video Amplifier

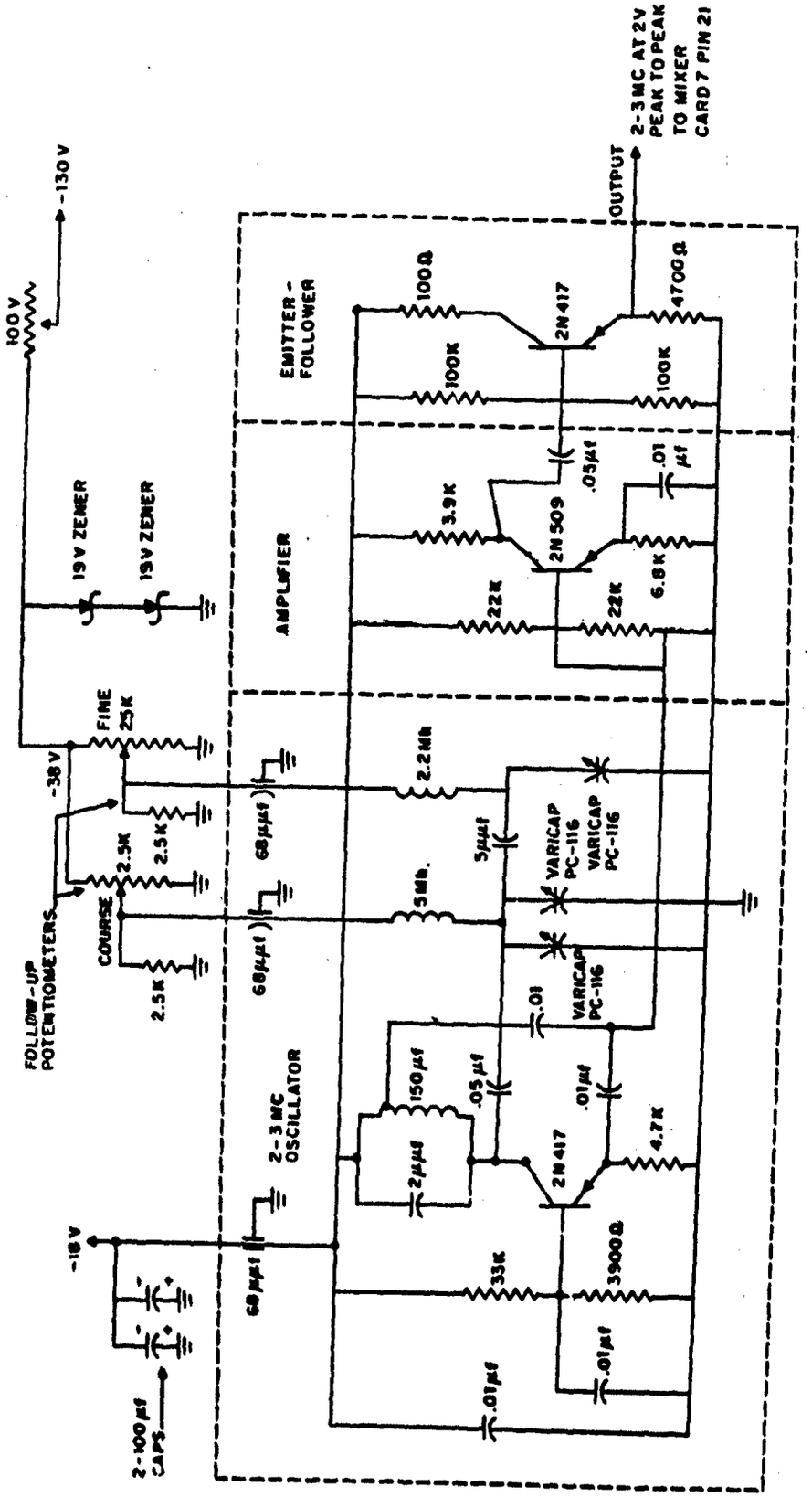


FIGURE 10 - Circuit Diagram - 2.0 to 3.0 mc VFO

U. S. Naval Air Development Center, Johnsville, Pa. Aeronautical Electronic and Electrical Laboratory

I. Halko, C.
II. Rawley, J.

FREQUENCY SYNTHESIZER, A METHOD OF FREQUENCY CONTROL BY DIGITAL CONVERSION; by C. Halko and J. Rawley; 18 Dec 1962; 19 p; Report No. NADC-EL-6272; Foundational Research Report, WEPTASK No. R360FR102/2021/R011-01-01, Task No. FR40-3-03(6105A).

A study was initiated to develop a frequency synthesizer to replace present day spectrum generators. The design objectives were to minimize spurious signal outputs, eliminate mechanical components, and to incorporate electronic circuitry compatible with micro-miniaturization techniques.

A method of frequency control was developed, using counters and logic circuits to develop a highly accurate coded error to connect to a variable frequency oscillator.

U. S. Naval Air Development Center, Johnsville, Pa. Aeronautical Electronic and Electrical Laboratory

I. Halko, C.
II. Rawley, J.

FREQUENCY SYNTHESIZER, A METHOD OF FREQUENCY CONTROL BY DIGITAL CONVERSION; by C. Halko and J. Rawley; 18 Dec 1962; 19 p; Report No. NADC-EL-6272; Foundational Research Report, WEPTASK No. R360FR102/2021/R011-01-01, Task No. FR40-3-03(6105A).

A study was initiated to develop a frequency synthesizer to replace present day spectrum generators. The design objectives were to minimize spurious signal outputs, eliminate mechanical components, and to incorporate electronic circuitry compatible with micro-miniaturization techniques.

A method of frequency control was developed, using counters and logic circuits to develop a highly accurate coded error to connect to a variable frequency oscillator.

U. S. Naval Air Development Center, Johnsville, Pa. Aeronautical Electronic and Electrical Laboratory

I. Halko, C.
II. Rawley, J.

FREQUENCY SYNTHESIZER, A METHOD OF FREQUENCY CONTROL BY DIGITAL CONVERSION; by C. Halko and J. Rawley; 18 Dec 1962; 19 p; Report No. NADC-EL-6272; Foundational Research Report, WEPTASK No. R360FR102/2021/R011-01-01, Task No. FR40-3-03(6105A).

A study was initiated to develop a frequency synthesizer to replace present day spectrum generators. The design objectives were to minimize components, and to incorporate electronic circuitry compatible with micro-miniaturization techniques.

A method of frequency control was developed, using counters and logic circuits to develop a highly accurate coded error to connect to a variable frequency oscillator

U. S. Naval Air Development Center, Johnsville, Pa. Aeronautical Electronic and Electrical Laboratory

I. Halko, C.
II. Rawley, J.

FREQUENCY SYNTHESIZER, A METHOD OF FREQUENCY CONTROL BY DIGITAL CONVERSION; by C. Halko and J. Rawley; 18 Dec 1962; 19 p; Report No. NADC-EL-6272; Foundational Research Report, WEPTASK No. R360FR102/2021/R011-01-01, Task No. FR40-3-03(6105A).

A study was initiated to develop a frequency synthesizer to replace present day spectrum generators. The design objectives were to minimize spurious signal outputs, eliminate mechanical components, and to incorporate electronic circuitry compatible with micro-miniaturization techniques.

A method of frequency control was developed, using counters and logic circuits to develop a highly accurate coded error to connect to a variable frequency oscillator.